

# *Printed Circuit Board FAQs*

## SCHWEIZER'S PARTNER NETWORK

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Schweizer Electronic AG stands for state-of-the-art technology and consultancy competence. SCHWEIZER's premium printed circuit boards and innovative solutions and services address key challenges in the areas of Power Electronics, Embedding and System Cost Reduction. Its products are distinguished

for their superior quality and their energy-saving and environmentally-friendly features. Together with its partners the company offers cost- and production-optimised solutions for small, medium and large series.



*Our partner for chip embedding*



**WUS Printed Circuit Co., Ltd.**

*Our partner for HF products in the automotive and industry segments*



**SCHWEIZER**  
ELECTRONIC



**MEIKO ELECTRONICS CO., LTD.**

*Our partner for reliable mass volumes and technology*



**ELEKONTA MAREK**  
Leiterplatten im Schnelldienst.

*Our partner for superfast prototypes and technology prototypes*

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## BASIC DATA



- ~ 770 Employees
- Plant area: 49 430 m<sup>2</sup>
- Production and logistic area: 33 200 m<sup>2</sup>
- 3-Shift production; currently 24/7
- Certificates
  - ISO 9001
  - TS 16949
  - ISO 14001
  - ISO 50001
  - EN 9100

	Standard / High End
Min. Conductor Line/ Space [µm]	75 / 50
Min. Microvia (laser drilling) drill diameter [µm]	110 / 100
HDI Build Up (Copper filled Laser Vias)	up to 3-x-3
Min. Mechanical drill diameter [µm]	200 / 150
Max. thickness PCB [mm]	2.4 / 3.8
Min. thickness PCB [µm]	500 / 400
Temp. Tg [C]	130 – 170 / 200 (HF 280)
Thermal conductivity base material [W/mK]	Data sheet supplier: 1.45 / 3.0 SCHWEIZER test method: 1.8 / 2.5
Solder mask	green, (white, black)
Surface finish	NiAu immersion. + galv. (fine and hard) NiPdAu (ENEPAG) OSP Immersion Tin HAL (SnPb and SnCuNi) Immersion Silver (via Subcon)
Max Size per PCB [mm]	575 x 583

# POWER ELECTRONICS

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Solutions in power electronics enable us to master the future challenges of electro mobility, energy creation and energy distribution.

In order to reduce fuel consumption as well as CO<sub>2</sub> emissions and to increase safety and comfort, it is increasingly necessary to switch higher currents and to dissipate heat.

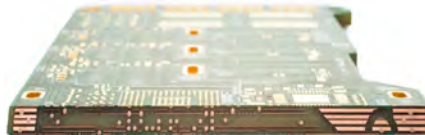
Amongst all PCB manufactures, SCHWEIZER offers the most comprehensive range of solutions to tackle these challenges. Already today, the automotive industry applies SCHWEIZER PCBs which can operate up to 1,200 Ampere.

## High Currents



Heavy Copper

## Logic & Power

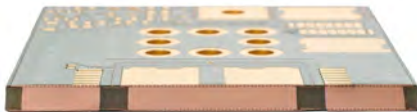


Power Combi Board

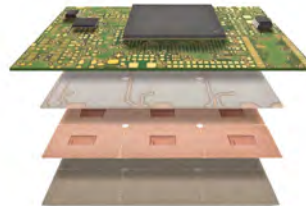
## Heat Dissipation



IMS Board



Inlay Board



p<sup>2</sup> Pack



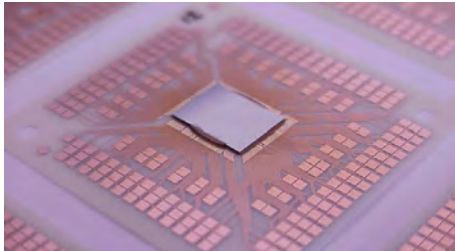
Cool Board

## EMBEDDING

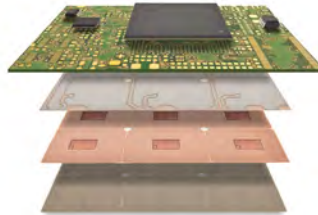
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Systems for many of today's and tomorrow's applications are subject to an advancing process of miniaturisation and have to offer additional functionalities at the same time. Examples are electric motors into which PCBs – together with the electronic system – are built.

In order to address the different individual requirements in the best possible way, SCHWEIZER developed a modular system for products and embedding solutions.



i<sup>2</sup> Board®



p<sup>2</sup> Pack®



μ<sup>2</sup> Pack®

## SYSTEM COST REDUCTION

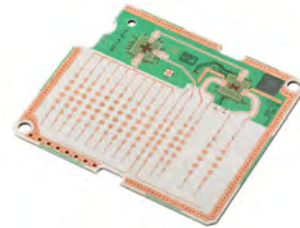
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A PCB is a relatively cheap component which, however, has a high relevance for the application. This requires balancing between cost on the one hand and quality and reliability on the other hand. A challenge that SCHWEIZER is meeting with.

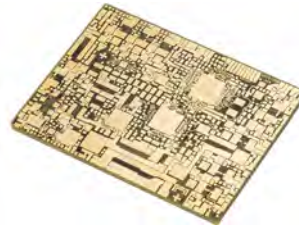
SCHWEIZER offers a variety of smart solutions. They contribute to reducing the overall system cost and thus also the cost of the entire system.



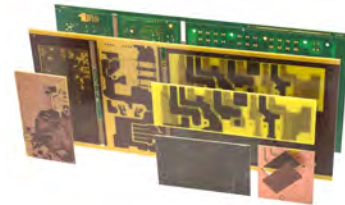
FR4 Flex



HF Board



Au wire bondable surface



All in one PCB

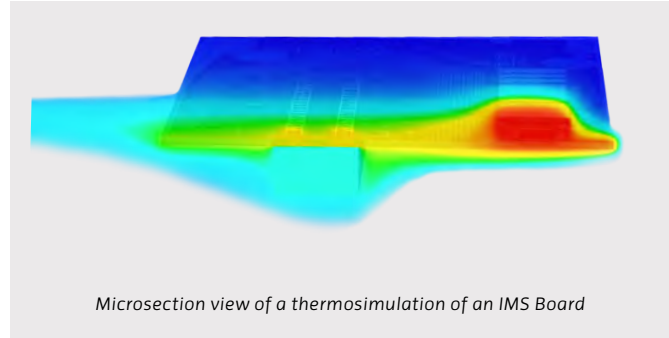
# IMS BOARD

## *For what applications are copper IMS most suitable?*

Copper IMS are deployed in many automotive- and industrial applications with higher power losses and/or currents. Besides high-power LED applications DC/CD converters and motor applications are preferred application fields. Based on the lower cost copper IMS are also utilised as a replacement for DCBs.

## *What is the meaning of IMS?*

The abbreviation IMS stands for “Insulated Metal Substrate”. Products utilising IMS technology are built up of a copper or aluminium back side metal sheet as a basis and one or more laminated copper- and base material layers. The IMS technology is very efficient for higher power applications featuring high power losses at limited layout density. Application examples are power-LED modules, DC/DC converters and motor control boards.

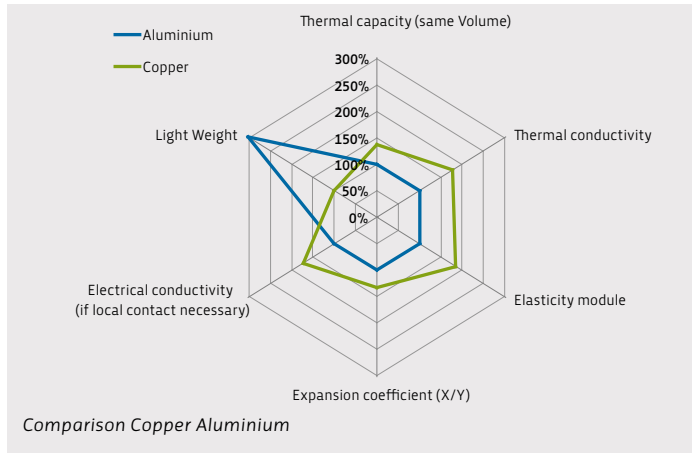


Microsection view of a thermosimulation of an IMS Board

## *Why is SCHWEIZER manufacturing copper IMS and no aluminium IMS?*

Unprotected aluminium substrates must not pass wet chemical PCB process steps due to bath contamination. Processing aluminium substrates does not match with highly automated PCB processes, which are part of SCHWEIZER's formula for success. Therefore SCHWEIZER is focussing on IMS technologies based on 1 mm copper substrates, other thicknesses on request. The material characteristics of copper offer many advantages in terms of thermal and electrical behaviour compared to aluminium. Furthermore the thermal expansion coefficient of copper (17 ppm/K) compared to aluminium (24 ppm/K) is advantageous especially to support highly reliable solder connections between the PCB and modern power LED packages based on aluminium nitride and sapphire substrates.





*Do I have to use a thermal interface material (TIM) to assure a sufficient heat transfer from the IMS to the heatsink?*

TIMs are thermally highly conductive materials which are e.g. employed to improve the heat transfer from the PCB to the heat sink. When deciding whether to use a TIM in the application or not, the engineer may consider that direct mounting of IMS onto the heatsink is a cost-efficient alternative. In many cases the thermal performance of direct mounted IMS is comparable. Besides the thermal resistance of the TIM itself based on material thickness and specific thermal conductivity, also thermal resistances of interfaces have to be considered.

*How many layers can be built up on the basis of a copper IMS substrate?*

Depending on the complexity of the circuitry SCHWEIZER is offering up to four electrical layers. The copper substrate does not count as electrical layer.



# FR4 FLEX TECHNOLOGY

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## *What is the FR4 Flex technology?*

FR4 Flex PCBs are rigid PCBs which are made bendable by means of a specially controlled deep routing process. The bending area is protected by a flexible solder mask instead of a standard resist. This flexible solder mask covers the copper traces without the generation of any cracks over life time. The bending area of the FR4 flex board can feature up to three electrical layers and can bend at angles from  $>0^{\circ}$  to  $180^{\circ}$ .

## *Where is the FR4 Flex technology utilised?*

When construction space is limited to two dimensions, the FR4 Flex technology is offering a third dimension for the PCB design. For instance, in many present electronic control units the contact area of multi-pin connectors is folded away by e.g.  $90^{\circ}$  to free up precious PCB area for other components. Generally FR4 Flex PCBs can be considered when construction space is prohibiting the use of a single rigid PCB and multiple bending cycles are not required.

## *What is the cost of FR4 Flex compared to rigid flex PCBs using polyimide foil?*

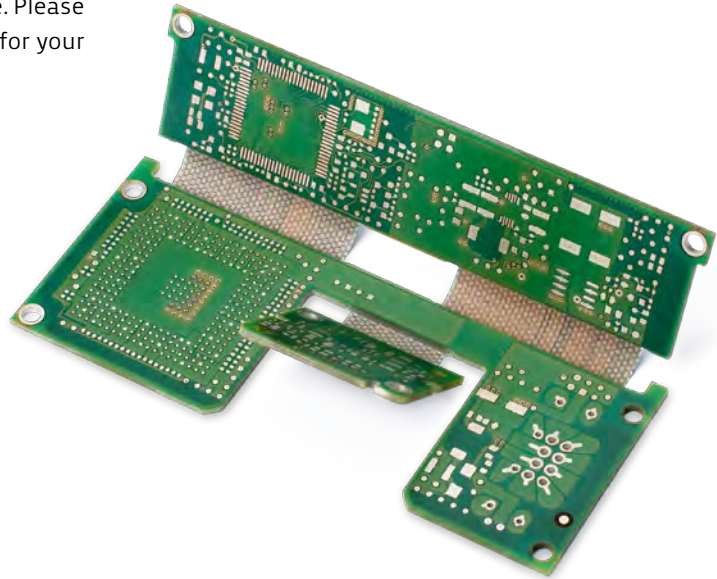
In comparison with rigid-flex PCBs with polyimide foil FR4 Flex is offering a distinct cost advantage. Depending on the lay-up savings of 30 to 50% are feasible. Moreover, process cost reductions are achievable since a pre-bake process is not required any longer.

## *Is FR4 Flex qualified according to automotive requirements?*

Yes, SCHWEIZER's FR4 Flex boards have been used for more than 15 years in automotive applications. More than 50 active parts with up to three electric layers in the bending area are currently manufactured for automotive customers. Among these are parts used in high-temperature environment or for safety-critical applications.

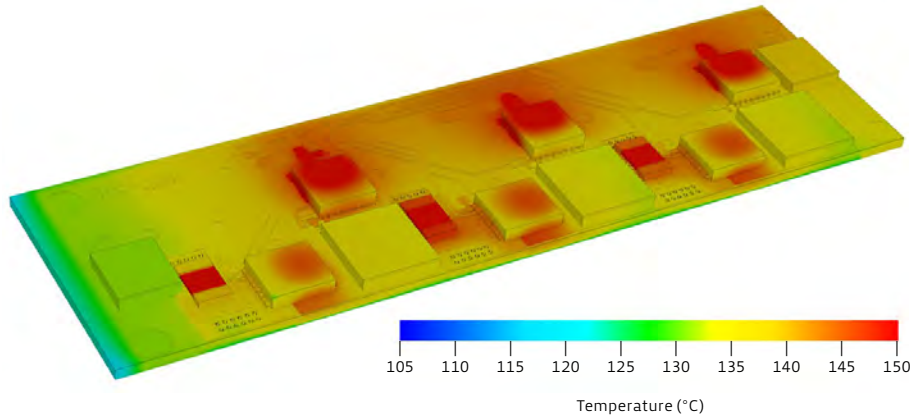
*How often can an FR4 Flex PCB from SCHWEIZER be bended and at what maximum bending angles?*

SCHWEIZER has developed dedicated test equipment for the qualification of the FR4 technology. In extensive test series a specification of maximum bending angles and the maximum number of bending cycles have been determined. Those values vary depending on base material combinations, prepreg type, thickness of copper cladding and mission profile. Please contact us. We will find an appropriate solution also for your 3D challenge.



## HEAVY COPPER TECHNOLOGY

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*Thermosimulation of a Heavy Copper PCB featuring 2 x 400  $\mu\text{m}$  copper on inner layers and 2 x 105  $\mu\text{m}$  on outer layers. Power dissipation of MOSFETs: 10 W each.*

*What is the difference between a Heavy Copper PCB and a Standard PCB?*

Generally Heavy Copper PCBs are manufactured with the same processes than standard PCBs. Inner layer thicknesses might vary between 105  $\mu\text{m}$  und 400  $\mu\text{m}$ . Etch trenches will be deeper and wider for Heavy Copper Boards compared to standard PCBs. Filling up those trenches requires sufficient enough prepreg material in order to generate the required amount of resin during the lamination process.

*How much current can be conducted by a Heavy Copper Board?*

Depending on the used active and passive components, the cooling concept of the application and environmental conditions like e.g. ambient temperatures solutions for continuous currents of up to 250 A are well-established.

### *Can laser vias be reliably connected to heavy copper layers?*

For conventional Heavy Copper PCBs laser vias cannot be utilised, since thick isolation layers lead to forbidden aspect ratios for the given laser hole diameter. For Heavy Copper PCBs mechanical depth drilling should be utilised.

### *How many Heavy Copper layers can be realised in a lay-up?*

The layer count is limited by the maximum PCB thickness of 3.2 mm and the weight limit for working panels. Accordingly, lay-ups with copper thicknesses of 4 x 400 µm, 6 x 210 µm or 10 x 105 µm of copper on inner layers are possible.

### *How can I contact a Heavy Copper board with a high-current connector?*

High-Current press-fit contacts are suitable for the conduction of high currents into and out of Heavy Copper lay-ups. They are available in different power classes and various connector geometries. Direct soldering or screw-mounting processes are not recommended in order to avoid reliability constraints.

### *Why are classical heavy copper boards insufficient for some types of applications?*

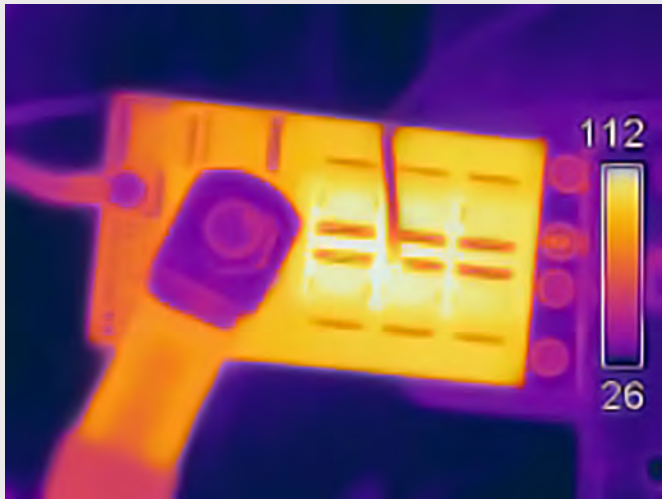
If applications require currents of a couple of 100 Amps whilst at the same time they have to dissipate high power losses, classical Heavy Copper PCBs are reaching their physical limits. Therefore SCHWEIZER is currently developing the Heavy Copper T<sup>2</sup> technology (T<sup>2</sup> = thinner & thermally enhanced). The target is a reduction of the thermal resistance of the PCB compared to classical heavy copper lay-ups by up to 50%.

## INLAY BOARD TECHNOLOGY

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*What is the maximum current that can be conducted by an Inlay Board?*

This depends on the possible conductor cross-section. At a maximum inlay thickness of 2.0 mm, continuous currents of 600 A and peak currents of 1,200 A are achievable. In each case, the exact value depends, of course, on the ambient conditions and the admissible power loss.



Thermography of a smart battery switch carrying 400 A permanent current (in collaboration with Infineon Technologies AG).

*How can contact be made with an Inlay Board?*

Inlay Boards are highly variable in terms of the contacting type. A partial exposure of contact surfaces allows screws and terminals to be attached and hard soldering or welding to be carried out. The use of press-in contacts is also common.

*What inlay thicknesses are possible?*

Depending on the application requirements, standard thicknesses of 1.0 mm, 1.5 mm and 2.0 mm are available.

*What forms and sizes can be mapped as inlay?*

Forming is quite variable and can be adjusted to individual application requirements. Depending on the dimension and complexity of the inlay parts, different solutions are available. We will be glad to advise you on the best solution for your application.

*Can an Inlay Board be laid up electrically insulated to make mounting toward the heat sink more economical?*

Basically, Inlay Boards exist in three different design versions:

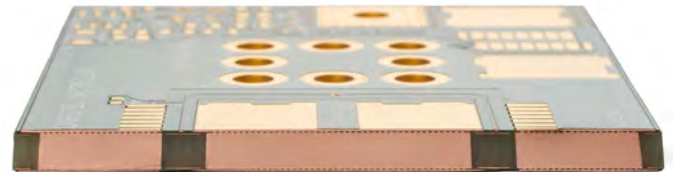
1. Open inlay – not insulated toward the heat sink.
2. Embedded inlay – with electrical and thermal connection to the outer layer via microvias.
3. Embedded inlay – insulated with thermally conductive dielectric.

*What functions can an inlay perform in a printed circuit board?*

1. Conducting high currents
2. Dissipating and discharging power losses
3. Counterpart for variable connection technology.

*How do printed circuit boards with pressed-in coins differ from the SCHWEIZER Inlay Board?*

Copper coins are only used for discharging power losses, thus performing only part of the function of the inlay technology. Coins are pressed into end-to-end printed circuit board holes and are usually round or rectangular in shape. The advantages of this technology are that they are usually low-cost and also allow contact to be made with inner layers. Compared with that, the Inlay Board has the advantage that the absence of a size limit allows heat dissipation over a large surface area. Since inlays can be laminated into the printed circuit board, no disruptions of the printed circuit board material can be caused by the pressing process, possibly limiting reliability. Compared with that, Inlay Boards have coplanar top and bottom sides simplifying the component assembly process.



## COPPER-FILLED THERMAL VIAS

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### *How deep is a dimple of copper-filled laser vias?*

Depressions of copper-filled laser vias which mostly result from unfavorable hole geometries are referred to as dimple. The dimple depth is 0 to 25  $\mu\text{m}$ , depending on the ratio of hole depth to hole diameter.

### *Can laser vias be directly connected to a copper inlay?*

The great advantage of the inlay technology is the connection of inlays with copper-filled laser vias. This can be used to achieve the thermal resistance of a PCB of  $<0.1 \text{ K/W}$ , for example by means of a bilateral connection of laser vias to an inlay.

### *What is the diameter of a copper-filled laser via?*

Laser vias which are used for the transmission of high currents and power losses have a diameter of 120  $\mu\text{m}$  – 160  $\mu\text{m}$  in standard applications.

### *What is the maximum thickness of the dielectric when using laser vias?*

The maximum insulation distance is calculated from the hole depth and the via diameter. The basis is an aspect ratio of 0.8:1. With a drilling diameter of 150  $\mu\text{m}$  and a copper thickness of 18  $\mu\text{m}$ , the maximum thickness of the dielectric remains 100  $\mu\text{m}$ .

### *How much power dissipation can be dissipated via laser vias?*

With optimum connection to the heat sink, with a via field of 9 x 9 mm, for example with 500 laser vias, it is possible to conduct up to 500 W power dissipation through the PCB with a  $\Delta T < 20\text{K}$ .



### *What electrical resistance has a thermal via?*

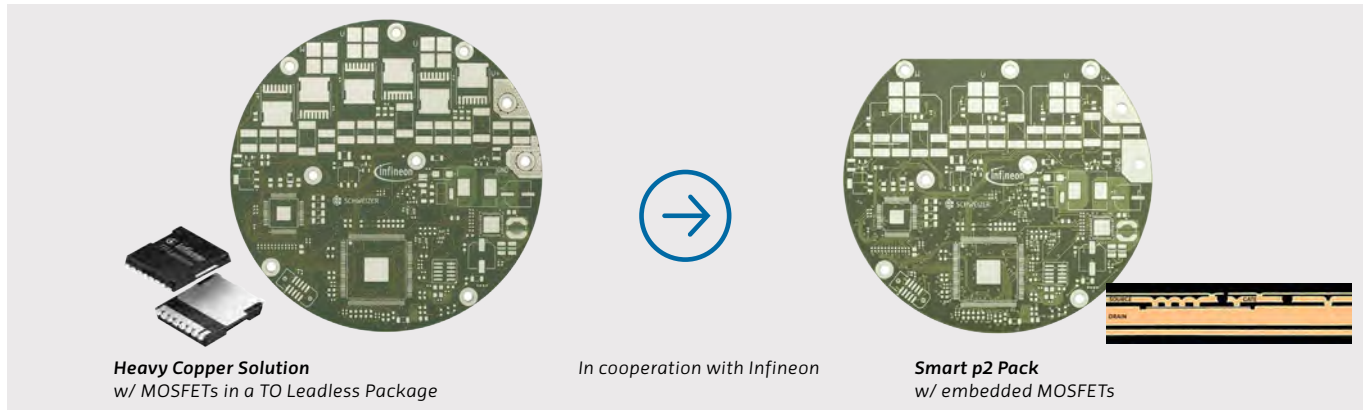
The electrical resistance of a copper-filled laser via depends on diameter and hole depth. With a typical diameter of 150  $\mu\text{m}$  and a hole depth of 100  $\mu\text{m}$ , a completely filled via has an electrical resistance of approx. 0.1 m $\Omega$ .

### *What is the minimum distance required for placing laser vias next to each other?*

For vias with identical potential, minimum web widths of 250  $\mu\text{m}$  can be implemented. For a via diameter of 150  $\mu\text{m}$ , the minimum distance (from hole center to hole center) is thus 400  $\mu\text{m}$ .

### *Why are laser vias completely filled if possible at SCHWEIZER?*

Completely filled laser vias allow direct soldering of power components on a via field. This direct type of heat dissipation offers great advantages in comparison with non-filled laser vias as in this case the heat must be spreaded first before it can be dissipated downward through the laser vias.



### What is the meaning of the abbreviation “p<sup>2</sup> Pack”?

The abbreviation p<sup>2</sup> Pack stands for “PCB Power Package” (p x p = p<sup>2</sup>). This technology can be used to embed power semiconductor modules for MOSFETs, IGBTs or Wide Band Gap semiconductors into the resin matrix of a PCB.

### What is a p<sup>2</sup> Pack and what is it used for?

A p<sup>2</sup> Pack is a PCB-based semiconductor package. Such as comparable modules, the embedded power semiconductors can carry out specific switching tasks in the different topologies. The p<sup>2</sup> Pack is used wherever applications with conven-

tional technologies such as packaged components or power modules reach their technological limits or are confronted with space problems.

### What is a p<sup>2</sup> Pack-DSV and what is it used for?

The abbreviation DSV stands for Double Sided Vias. In this technology, the chip contact surfaces are connected directly to the laser vias. The p<sup>2</sup> Pack DSV is used in the medium output category which is not focused on maximum performance in heat dissipation and current carrying capacity but on a compact design.

### *What is a Smart p<sup>2</sup> Pack?*

The p<sup>2</sup> Pack is a real power module where high currents are transferred through thick-copper layers. This semiconductor power module will be integrated in a logic board. This will create a PCB which offers both power and logic circuits. This combination is called a Smart p<sup>2</sup> Pack.

### *What are the advantages of the p<sup>2</sup> Pack?*

#### **Optimised assembly and connection technology**

The DCB power electronics substrate and the logic board are now combined to give a PCB. This makes cables and plug-in connectors superfluous and improves reliability.

#### **Improved contact resistance of the power electronics**

Since in the p<sup>2</sup> Pack bondwires are replaced with copper-filled vias and the chip is then contacted on the surface of the top side, the forward power loss is reduced. The exact value depends on the particular technology generation of the semiconductor, the voltage class used and the semiconductor package to be compared.

#### **Improved thermal resistance**

The excellent heat spreading of the Smart p<sup>2</sup> Pack allows the

overall RTH of the system to be significantly improved. First demonstrators have even shown advantages over DCB ceramics, even though DCB, for example with Al<sub>2</sub>O<sub>3</sub>, has a heat conductivity of 24 W/mK and the p<sup>2</sup> Pack works with prepegs, which only have 1.85 W/mK. In the future, optimised prepegs will be available, which will reinforce this advantage further.

#### **Low-inductive design**

The p<sup>2</sup> Pack allows primary dc-link capacitors or snubber networks to be taken significantly closer to their output stage, thus significantly reducing voltage overshoots during switching. Previous demonstrators have shown a decrease in parasitic inductance of up to 85%.

#### **Improved switching behavior and more rapid switching possible**

The almost superficial connection of the chip top side to the vias allows quicker switching, resulting in smaller passive components being required, thus saving system costs.

Moreover, the p<sup>2</sup> Pack shows significantly fewer overshoots during switch-on and switch-off. This results, for example, in 48 volt systems being usable nowadays with 80 V MOSFETs and no longer requiring a 100 volt junction voltage. 80 volt MOSFETs have a correspondingly lower  $R_{DS(ON)}$ . A smaller  $R_{DS(ON)}$  and lower switching losses lead to a lower power loss, thus clearly lowering the maximum chip temperature with the same

operating mode. It is up to the user whether he/she wants to use this advantage for a longer life, a lower cooling system expenditure or for a lower chip size.

### **Improved electromagnetic compatibility (EMC)**

The fact that the power electronic semiconductor is shielded by two copper layers improves the electromagnetic compatibility. This should make it possible to reduce the EMC protective measures. This affects only some applications. Here it is up to the customer to decide to what extent this advantage is relevant for him.

### **Built-in insulation**

As a general rule, today thermal interface materials (TIM) are used between the PCBs and the heat sinks. They usually have a heat conductivity of approx. 2 W/mK. However, this value often lowers the overall performance of the design. Since the p<sup>2</sup> Pack is already insulated, other optimised TIM of 2–20 W/mK can be used, which should significantly improve overall performance.

### **Miniaturisation**

Many systems for today's and future applications must get smaller and smaller and, at the same time, provide additional functionalities. The p<sup>2</sup> Pack technology allows valuable space to be saved already in the PCB solutions. In the demonstrator

shown, developed by SCHWEIZER together with Infineon, the size of the PCBs for the accessory drive, for example, could be reduced by approx. 15 percent compared to conventional solutions.

### **Increased reliability**

The use of bonding wires or DCB ceramics substantially increases reliability. In thermal cycle tests with a temperature differential  $\Delta T$  of 120 K, designs were able to master more than 700,000 active cycles.

### **Reduction in system costs**

The saving of plug-in connectors and cables, lower cooling measures, the reduction in the required chip surfaces of the power components, smaller passive components, reduced EMC measures and the insulation already in place, as well as the saving of space overall result in a significant saving of system costs.

*Which currents could be achieved with the p<sup>2</sup> Pack technology?*

Depending on the semiconductors used and the performance capability of the cooling system, continuous currents of 400 amperes can be transferred.

*How many logic layers can be realised in a Smart p<sup>2</sup> Pack?*

6 logic layers are reasonable. But even more layers can be realised.

*When will the first p<sup>2</sup> Packs be available?*

We have scheduled the series start of the technology in dedicated projects for 2019/2020.

*How will the p<sup>2</sup> Pack be integrated in the PCB design?*

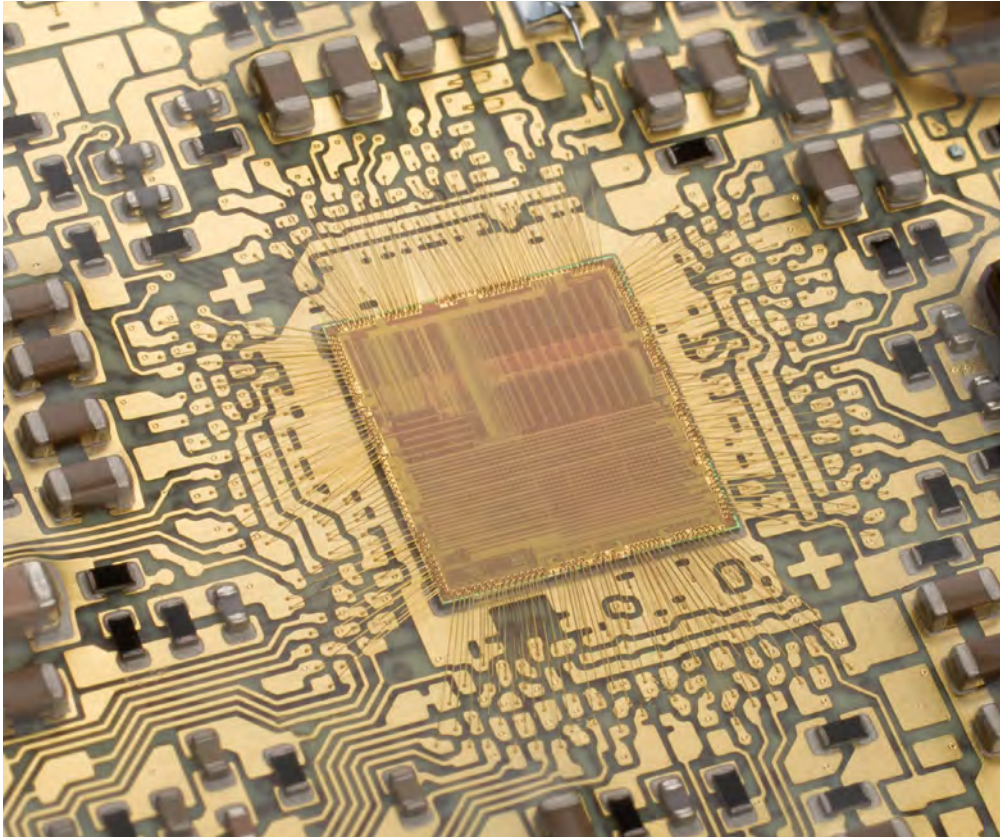
SCHWEIZER has established design guidelines for the development of the p<sup>2</sup> Pack technology. During the construction phase of a PCB using the p<sup>2</sup> Pack technology, we will support your development team. The implementation in the planning tool does not require special plugins.

*What are the costs for the p<sup>2</sup> Pack technology compared to modules?*

The costs for the p<sup>2</sup> Pack technology cannot be compared directly with a module. The costs for the entire system must be considered. In the entire system, we expect a reduction of the system costs (see question “Advantages of the p<sup>2</sup> Pack”).

## SURFACE FINISHES

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Bare Die HDI PCB with ENEPAG surface finish in cooperation with Continental AG

*What surface finishes are being offered by SCHWEIZER?*

SCHWEIZER is offering the following surface finishes:

- chemical tin,
- ENEPAG (Electroless Nickel Electroless Palladium Auto-catalytic Gold),
- HAL (Hot Air Levelling),
- OSP (Organic Surface Protection),
- chemical nickel-gold (ENIG, or Electroless Nickel Immersion Gold ),
- chemical and galvanic silver (provided by subcontractor),
- galvanic hard gold or fine gold.

### *For what purposes are the surface finishes being used?*

- **ENIG:**  
for aluminium wire bonding and/or as high-quality surface finish for soldering via paste printing,
- **ENEPAG:** for gold wire bonding,
- **chemical tin:**  
as standard surface finish for soldering via paste printing,
- **HAL:**  
soldering surface which carries the solder as a depot,
- **OSP:**  
most favourable surface finish for soldering via paste printing,
- **galvanic hard gold:**  
for mechanical sliding areas or plug-in contacts.

### *What storage time can we guarantee for what surface finish?*

SCHWEIZER always guarantees a solderability of 6 months for all surface finishes. With proper alignment of the storage conditions and for certain surface finishes, we can guarantee up to 12 months.

### *What is the difference between ENEPAG and ENEPIG?*

#### **ENEPAG:**

Electroless Nickel – Electroless Palladium – Autocatalytic Gold

#### **ENEPIG:**

Electroless Nickel – Electroless Palladium – Immersion Gold

In the ENEPIG process, gold is deposited on the surface in an exchange reaction. This exchange reaction produces different layer thicknesses on the different pad sizes. This makes it difficult to perform gold wire bonding. ENEPAG is a reductive gold deposition process that produces a homogeneous layer distribution of the gold layer. Therefore, this surface is ideally suitable for gold wire bonding.








### *Why is SCHWEIZER using ENEPAG for gold wire bondable surfaces instead of ENEPIG?*

The surface in the ENEPAG process has a purer gold surface, which is required for bonding. Over the course of the process, the layer thicknesses can be achieved more quickly and more homogeneously. The comparable gold process would be galvanic fine gold, which is more complex and more expensive to produce, hence applying the ENEPAG process results in a cost reduction for our customers.

### What is the difference between galvanic fine gold and hard gold?

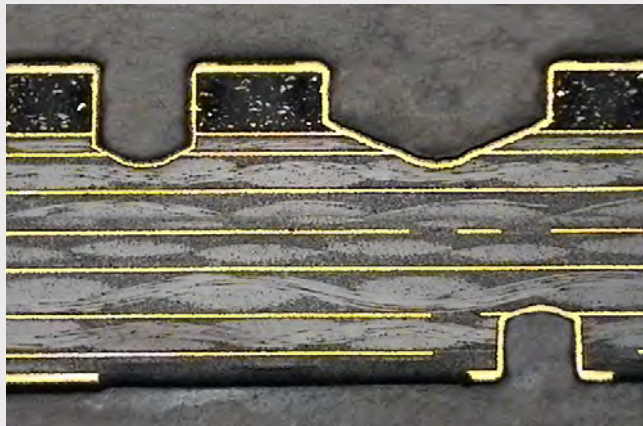
Fine gold is 99.99% pure gold, while hard gold is an alloy containing cobalt and making the gold harder and more abrasion-resistant. Fine gold is used as an alternative for gold wire bonding surfaces, while hard gold is used for mechanical requirements.

### Which layer thicknesses can be produced?

Final surface	Hard gold	Fine gold	Imm. NiAu (ENIG)	Imm. NiPdAu (ENEPAG)	Imm. Sn	HAL	OSP	Imm. Ag
Description	galv. Nickel / Gold for contacts	galv. Nickel / Gold	Nickel-Phosphorus / Gold	Nickel-Phosphorus / Palladium / Gold	Tin-Silver	Sn alternatively Sn-Pb 63/37	passivated Cu	Silver
In-House Process								via subcon
Layer system	Au 0.5 – 1.5 µm	Au 0.5 – 1.5 µm	Au 0.05 – 0.1 µm	Au 0.03 – 0.08 µm	Sn >0.8 µm (1x soldering)	1 – 40 µm (non-planar)	passivated Cu ca. 0.2 – 0.4 µm	Ag 0.1 – 0.3 µm
	Ni 3 – 8 µm	Ni 3 – 8 µm	Ni 3 – 7 µm (soldering) Ni 4 – 8 µm (bonding)	Pd 0.1 – 0.3 µm Ni 3 – 8 µm	Sn >1.0 µm (2x soldering)			



## RADAR PCBS



Cross Section of a Radar PCB

### *What are the functions of a radar PCB?*

A radar PCB usually contains two antennas that are incorporated in the circuit pattern as etched copper structure. One of them is the transmitter and the other the receiver of radar waves. A radio-frequency circuit generates the waves and analyses the reflected signal. The entire function of the RF circuitry is based on special base materials that are capable of transmitting this radio-frequency radiation to the antenna with as little damping as possible and radiate it. The RF signals are analysed by a digital circuit located in modern radar

sensors frequently on the back of the PCB. The front of the PCB contains the complete RF part of the circuit, including the antenna structure.

### *What is the definition of a radar PCB?*

Radar PCBs are electronic circuits that are capable of producing and receiving radio frequency signals. They are based on special RF base materials. The entire circuit generates a so-called radar lobe, which is sent by the antenna structure of the PCB, then reflected by objects and received again by the antenna structure of the PCB.

### *In what applications are radar PCBs used?*

Radar PCBs are often encountered in automotive applications. More and more, radar applications are also used in the industrial sector and in building automation, such as in level meters, track monitoring or for automated door openers.

### *What is the concrete function of radar PCBs?*

Radar PCBs are used for the detection of speeds, measurement of distances and detection of objects. In the automotive sector, there are two different frequency bands. In close-range applications of typically up to 30 m, frequencies around 24 GHz are used, while in long-range applications of up to 200 m, frequencies range from 77 to 79 GHz.

### *What functions are performed by radar PCBs especially in the automotive sector?*

In the automotive sector, radar PCBs are used in a wide range of applications, such as, among other things, adaptive cruise control, autonomous emergency braking, collision mitigation, stop-and-go assistant, lane change assistant, lane departure warning system, blind spot detection, cross traffic alert, rear parking aid, and a few more. In the future, the use of several radar sensors will become the standard in vehicles with fully or even only partially automated driving. The higher the degree of automation, the higher the number of radar sensors required.

### *Why is SCHWEIZER well prepared for the challenges of radar PCBs?*

For modern radar systems, currently so-called hybrid assemblies are often being used. This is understood as a combination of FR4 and RF base materials. Due to their special transmission properties of radar signals, RF base materials are five to ten times more expensive than FR4 base materials and show clearly different processing properties. Thanks to its more than ten years of experience in radar applications, SCHWEIZER masters the challenges of these material combinations. For example, the specifications for warping and twisting the PCB present a much greater problem than with standard FR4 PCBs. Moreover, the low tolerances of the conductor track and antenna geometries are often near the limit of the options available with modern PCB processes. SCHWEIZER has optimised the entire process chain with a view to the applications described, making radar PCBs nowadays a core competence of SCHWEIZER. SCHWEIZER is world market leader in the segment of automotive radar PCBs. In addition, with WUS, SCHWEIZER has a very well experienced and good cooperation partner in Asia in order to provide the necessary capacity for the strong market growth.

*Why are radar PCBs much more complicated to manufacture in the frequency range 77–79 GHz compared with the 24 GHz range?*

Owing to their wavelength, which is approximately two thirds lower, antenna structures and conductor geometries must be designed correspondingly smaller and manufactured within significantly narrower tolerance limits. At the same time, teflon-based base materials are often used, which are more difficult to process not only due to the high hardness of the fillers, but also due to their clearly lower stability. The reliability requirements of the end products increase driven by their usage in safety-critical areas. Since an increasing number of sensors must do with less and less space, the integration density of the circuit in combination with high power losses increases as well. Here SCHWEIZER's embedding technologies reveal ways for future system solutions.

*Why is long-standing experience in the manufacture of radar PCBs a great advantage for a PCB manufacturer?*

The use of special RF base materials in conjunction with standard FR4 base materials and their highly advanced processing require many years of development and experience in high-volume manufacture of these products. Our customers value this experience and integrate SCHWEIZER into the development process early on, in order to substantially shorten the development period and start volume production using stable production processes.

# POWER COMBI BOARD

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## *What does SCHWEIZER understand by Power Combi Board?*

SCHWEIZER understands the Power Combi Board to mean a combination of a power part with copper layer thicknesses up to 400  $\mu\text{m}$  on inner layers and a logic part with usually 35  $\mu\text{m}$  on inner layers, while the number of layers in the logic part is usually higher. Thus, the logic part can be manufactured as a 6-layer board, while the power part has only 4 layers. The electrical connection between the two parts is provided via the mutual outer layers.

## *How is the Power Combi Board manufactured?*

In the power part, the heavy copper technology is applied to manufacture the pre-structured inlay part. This heavy copper inlay is placed into an FR4 frame featuring matching cavities. The layup is completed by commonly used prepregs and copper foils on the upper and lower side. In the subsequent lamination process, the logic and power parts are combined to the Power Combi Board.

## *What technical advantages does a Power Combi Board offer for the application?*

Designers of power applications frequently face the challenge of placing increasing functionality and performance within an ever decreasing volume. As a result conventional strategies, such as separation into a power and a logic board or use of a logic board in combination with lead frames or DCBs, are hardly expedient. The Power Combi Boards enable the integration of complete functional groups, minimisation of the required volume and improvement of the system reliability by a considerable reduction of screwed, clamped and soldered connection points.

### *Does a Power Combi Board have commercial advantages?*

Apart from the technical advantages, a Power Combi Board can also help to lower cost. Essential is the size of the power part compared to that one of the logic part. Generally speaking, the commercial advantage is significant when the area percentage of the logic part exceeds that of the power part.

### *Which applications are ideal for the use of the Power Combi Board?*

Suitable applications are the ones requiring compact ECUs which are operated in the power part at continuous currents of more than 80 A and simultaneously require a complex logic. Among those applications are e.g. motor control ECUs and voltage converters.

### *What are the concrete advantages that a Power Combi Board has in comparison with a conventional heavy copper PCB with 400 µm copper thickness in the inner layers?*

The conventional heavy copper PCB significantly limits the layout design of logic structures even if they are only present on the outer layers. This is due to the design rules for 400 µm

copper layers which do not allow a net distance below 2.5 mm. In the Power Combi Board, the power and logic structures are located next to each other so that the logic part is not subject to such restrictions. Altogether, this makes it possible to reduce the logic part significantly and decrease the required total available space of the application.

### *Can the Power Combi Board technology also be combined with other technologies?*

The demonstrator on the picture shows the combination of two SCHWEIZER technologies. The high current part for the three-phase fan motor control is located in the area of the Power Combi Board technology (image foreground). Use of the FR4 Flex technology allows to position the logic part of the PCB at a defined angle to the high current area. Thus, logic and power can be placed within the available space for a control unit in the most space-saving way.

# IMPEDANCE

## *What does impedance mean?*

### **Technical definition** (source: German wikipedia):

Impedance, also referred to as alternating current resistance, is the ratio of electrical voltage at a consumer (component, cable, etc.) to current consumption. In general, this physical variable is advantageously expressed as a complex-valued function of the frequency.

From the point of view of the PCB manufacturer, impedance adjustment is a complex requirement. A large number of PCB parameters have a direct effect on impedance, which is why they must be manufactured to very low tolerances.

## *Which requirements must an impedance PCB fulfil?*

- Base materials and prepregs have been defined,
- Layer assembly is impedance-adjusted,
- Signal routing complies with impedance models,
- Signal tracks have been marked,
- Reference planes have been clearly assigned,
- Nominal values and tolerances of the impedance have been determined.



## *What effect does the selection of the PCB manufacturer have on impedance?*

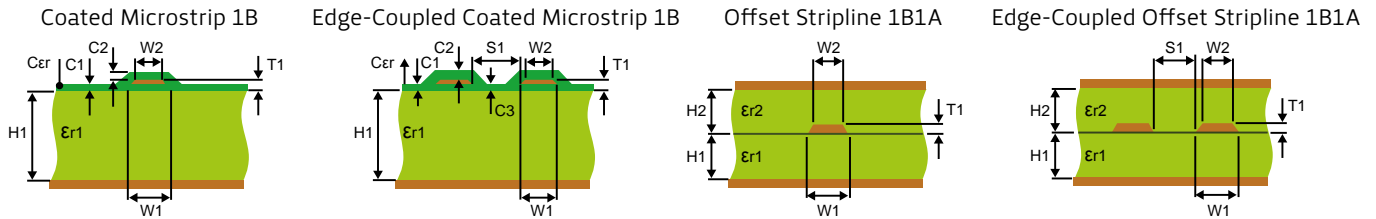
The selection of the manufacturer can have far-reaching effects on impedance, as different manufacturers tend to prefer different base materials and constructions.

Impedance PCBs must be coordinated with the manufacturers beforehand. Changing them without prior coordination involves great risks for the impedances obtained.

## *What tolerances are commonly used?*

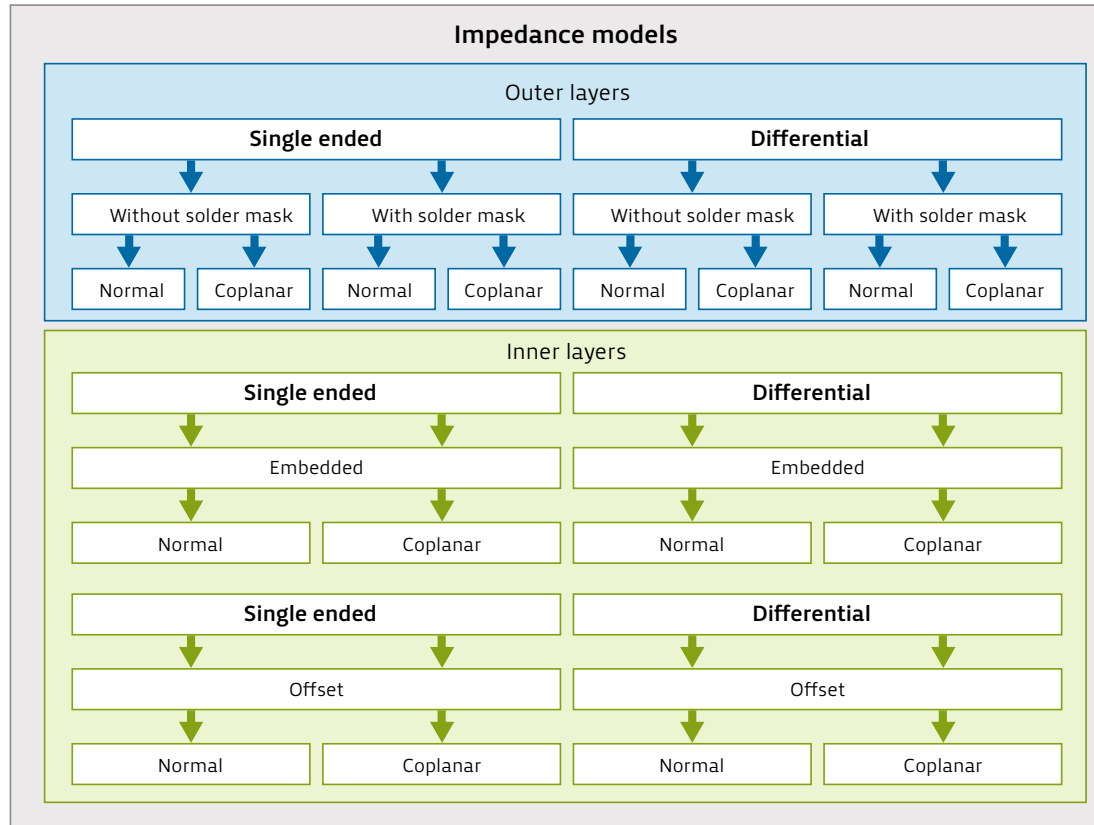
Common tolerances are  $\pm 10\%$  of the rated value of the impedance. In principle, lower tolerances are possible, but require precise evaluation.

Which PCB processes have an effect on impedance?



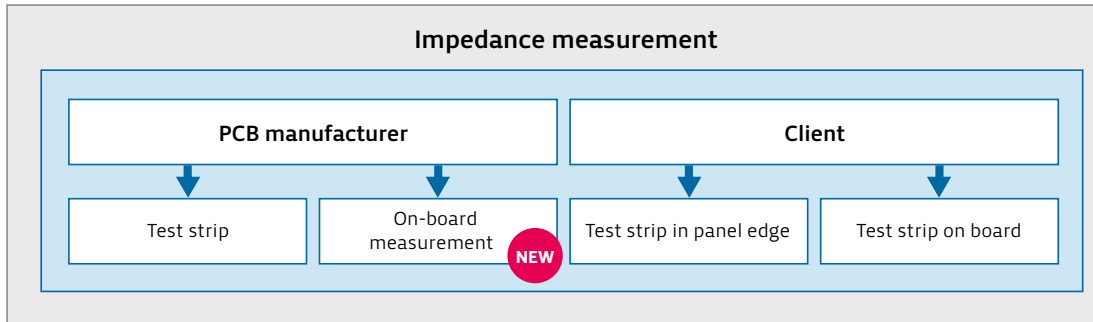
Abbreviation	Description	PCB technology / influence factors
$\epsilon_{r1}$ , $\epsilon_{r2}$ , $C_{\epsilon r1}$	Dielectric constant	raw material (base material prepreg, solder mask)
$C_1$ , $C_2$ , $C_3$	Layer thickness solder mask	raw material (solder mask) → coating process
$T_1$	Layer thickness copper	outer layers (base copper + galvanic build-up) → galvanic process inner layers (base copper) → etching process
$W_1$ , $W_2$	Track width	etching process
$S_1$	Track distance	etching process
$H_1$ , $H_2$	Dielectric thickness	raw material (base material + prepreg) → multi layer pressing
	Condition of reference plane	etching process; copy accuracy
	Drilling technology	aspect ratio; blind via technology, buried vias, back drilling

*Which impedance models can be used?*



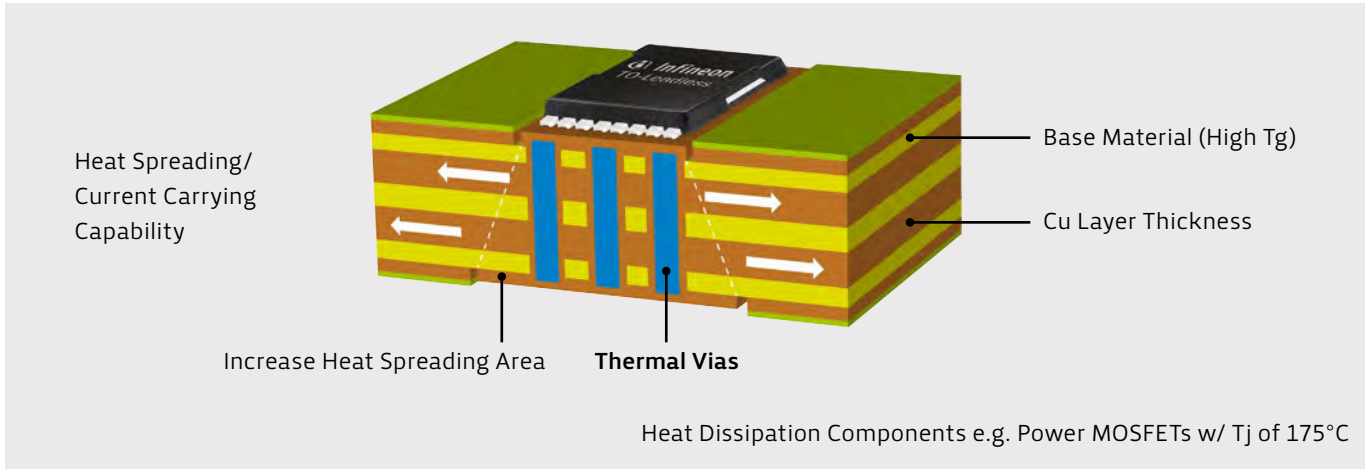


### How and where is impedance measured?



An impedance is measured using the TDR (Time Domain Reflectometry) measurement method. There are four ways of measuring impedance. The traditional variant is the test coupon adjusted by the manufacturer to the PCB conditions and placed in the production panel. Customers can implement test structures in the panel edge or directly on the PCB. In addition, differential impedances can also be measured directly.

## THEMAL VIAS



*What significance does the number of copper-plated holes and the thickness of copper plating in these holes have for the thermal performance of the PCB?*

The greater the mass of copper that can be placed under heat-generating components or in their direct vicinity, the better will be the dissipation of heat from their underside. In the case of heat dissipation with plated-through holes, both their number and the thickness of their copper layer are crucial in the thermal performance.

*How does the thermal resistance of a four-layer stack up with 2x 400  $\mu\text{m}$  copper foils on the inner layers compare to a ten-layer stack up with 8x 105  $\mu\text{m}$  copper? Both stack ups have a comparable overall thickness of copper in the inner layers and the same configuration of thermal vias.*

The thicker the insulating layer in the overall stack up, the greater the thermal resistance will be, because FR4 material (0.4 W/mK) represents a thermal barrier compared to copper (400 W/mK). If two 400  $\mu\text{m}$  Heavy Copper layers are replaced by eight 105  $\mu\text{m}$  copper layers, a greater thickness will be required for the insulation layers overall. Despite the same

total mass of copper, the PCB becomes thicker as a result, which in turn leads to deterioration in thermal resistance. In the case of classical 400 µm Heavy Copper technology, the overall thickness in the sample PCB is 2.0 mm and hence 0.3 mm thinner than the PCB using 105 µm Heavy Copper technology. This advantage is reflected in a 15% lower thermal resistance. The difference to the Heavy Copper T<sup>2</sup> technology currently developed by SCHWEIZER is even greater.

*How does the thermal resistance change with a constant number of vias due to a reduction in the PCB thickness with the aid of Heavy Copper T<sup>2</sup> technology?*

Heavy Copper T<sup>2</sup> technology is being developed by SCHWEIZER in order to achieve additional benefits in thermal behaviour compared with conventional Heavy Copper technology. The decisive lever is the reduction of the insulation layer, which is almost impervious to heat, by approx. 50%. Despite the placement of CNC-drilled, copper-plated thermal vias for heat dissipation of the power components, a reduction in the thermal resistance of more than one third of the initial value is achieved in the application typically investigated.

*What is the minimum distance between the hole walls of two CNC-drilled thermal vias?*

The minimum distance depends on the overall thickness of the PCB and the base materials used. The resulting minimum distance from hole wall to hole wall (without metallisation) is typically between 0.2 mm and 0.5 mm.

*Is the plugging and capping of vias an economically meaningful method of reducing the thermal resistance of a PCB?*

Closing through-holes with plugging paste (thermal conductivity approx. 0.5 W/mK) produces practically no improvement in thermal resistance as the power losses take the path of least thermal resistance so that only the cross-section of the copper barrel functions as a heat conductor. However, plugging in combination with capping becomes indispensable with a high density of plated-through thermal vias so that a sufficiently large soldering area can be made available.

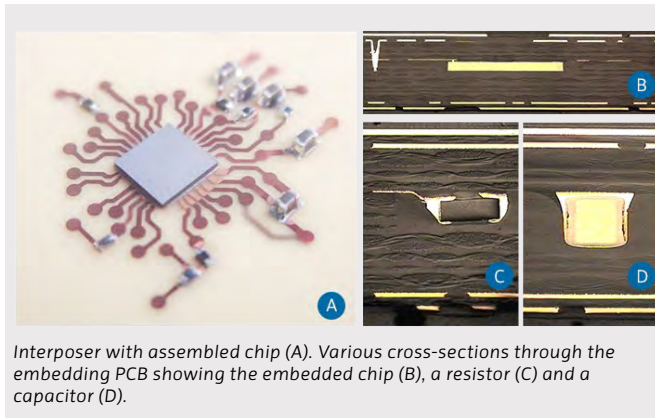
*What has to be observed in the neighbouring layout area of the thermal vias in order to ensure good heat dissipation?*

Coupling inner layers to plated-through thermal vias creates a spreading effect that additionally reduces the thermal resistance. A crucial factor here is the overall copper mass (thickness + area covered). The layout of the outer layers towards the heat sink has an especially large influence. This area should be designed as generously as possible in order to exploit the spreading effect to the best possible extent.

*Should solder mask be applied to the thermal vias on the side facing the heat sink?*

Normally the PCB is connected with the heat sink via a thermal interface material (TIM). The TIM not only guarantees the transport of heat to the heat sink but also represents an electrical insulation to the PCB and hence to the thermal vias on the rear of the PCB as well. Consequently, the function of the solder mask as an electrical insulator is not required in this case. From the thermal aspect, it is disadvantageous to overprint thermal vias with solder mask as the thermal resistance of the thin solder mask layer, due to its poor heat conductivity, is of a similar magnitude to that of the TIMs. Nevertheless, there are applications that demand overprinting with solder mask in order to minimise the risk of short circuits due to metal particles.

# LOGIC EMBEDDING



Interposer with assembled chip (A). Various cross-sections through the embedding PCB showing the embedded chip (B), a resistor (C) and a capacitor (D).

## Which logic components can generally be embedded into the PCB?

Nearly all logic components can be embedded into the PCB.

Exceptions:

- Semiconductors based on low-k dielectrics as substrate material,
- Chips in which the pitch of the electrical contacts  $< 80 \mu\text{m}$ ,
- Optical components (for obvious reasons).

## Under what conditions does it make sense to embed passive components?

It always makes sense to embed passive components when they support the function of the embedded component, such as in the case of block capacitors or terminating resistors.

## What advantages does embedding offer?

The embedding of components offers many advantages. The most obvious advantage is the saving of space on the assembly side because both the IC and the direct layout on the top side can be relocated to an inner layer. Due to the possibility of routing to layers situated both above and below, in certain conditions it may also be possible to reduce the complexity or layer count of the PCB. Furthermore, the heat dissipation of the IC also improves as the power loss is now no longer distributed via the soldering area and to a slight degree via convection but, instead, three-dimensionally with significantly improved heat transfers inside the PCB. The electrical behaviour may also exhibit a positive change due to the embedding of the IC. Shielding of the electromagnetic radiation is already ensured due to the technology used by the copper layers above the chip.

If required, IP protection can also be realised. The application can be implemented so that certain IC connections can only be accessed from outside by means of extremely complex preparation of the PCB.

The advantages of the embedding technology should be assessed individually and viewed in relation to a conventional solution. This is the only way to reach a meaningful decision regarding the optimum assembly and connection technology for the application.

#### *Can packaged semiconductors also be embedded?*

Yes, in principle. However, it is important to remember that the embedding of packages removes a number of application benefits compared with the embedding of semiconductor chips. Furthermore, the process is technically more complex and thus also incurs higher costs.

To summarise, SCHWEIZER advises against the embedding of package components for series production.

#### *What limits apply today in terms of chip size and the number of electrical contacts for a chip?*

As a matter of principle, it is technically feasible to embed both very small and simple chips as well as large and highly complex chips.

Due to the current cost structure and available production equipment for series production, there are, however, limits for the embedding of semiconductors that apply individually to each chip technology. The largest semiconductors to be embedded have an area of approx. 15 to 20 mm<sup>2</sup> and a number of contact pads ranging between approx. 150 and 200.

#### *How do semiconductor chips have to be reworked so that they can be embedded?*

This depends on the application and the assembly and connection technology employed. For components already provided with gold stud bumps, prototypes can be set up without any reworking. There are various options for use in series production such as nickel-gold under bump metallurgy (UBM), solder balls or even copper pillars with solder cap.

### *What challenges does the supply chain face?*

The use of embedding technology demands openness from the partners involved in the supply chain in order to adapt the traditional business model of the electrical industry. Usually the manufacturer of the electronics purchases the PCB, active and passive components as well as additional components. These are then assembled in an SMT soldering process to form an electronic module.

In the embedding model, a workable business model has to be drawn up between the manufacturers of the PCBs and the semiconductors in close cooperation with the customer. The business model has to regulate the purchase of wafers, their reworking and mounting as a flip chip on an interposer, the electrical test, the joint qualification process and the quality requirements. In addition to adherence to the specifications within the series, automotive and industry customers also demand a carefully devised quality concept and, in the event of returns, clear responsibilities from the partners involved.

### *What is the difference between i<sup>2</sup> Board® (i<sup>2</sup> = integrated interposer) and μ<sup>2</sup> Pack® (μ<sup>2</sup> = μ-thin / μ-pitch)?*

In PCB embedding technologies, a distinction is made between two fundamental approaches. Firstly the “System in PCB” approach, in which components are integrated into the main circuit board. In the “System in Package” approach, a semiconductor package is produced with the aid of PCB and embedding technologies which is then placed on a main circuit board. The i<sup>2</sup> Board® is one of the “System in PCB” solutions while the μ<sup>2</sup> Pack® adopts the “System in Package” approach.

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