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# Conducting Very High Currents through PCB Substrates at High Ambient Temperatures

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SCHWEIZER ELECTRONIC AG

# Introduction

One of the major challenges of our time is climate change and the associated need to reduce greenhouse gas emissions. The requirement to reduce  $CO_2$  emissions has brought about significant changes in the area of power generation, and also in the area of mobility.

Supported by a favorable subsidy policy, the solar boom originated in Germany and quickly spread widely across Europe. Government policy has specified a sharp reduction of  $CO_2$  emissions for the automotive industry as well, increasing the pressure to come up with new developments within the entire supply chain.

The advancing electrification of motor vehicles that currently takes place predominantly in the area of auxiliary units, and the demand for power inverters for renewable energy sources, have triggered a worldwide demand for power electronics components and led to significant development efforts towards efficient, cost-effective and reliable power electronics.

### **Challenges in Power Electronics**

Anyone in the field of power electronics will quickly get involved in discussions about efficiency. On the one hand, the reasons result from technical requirements and, on the other hand, from purely economic considerations. For example, the efficiency of a solar power inverter to be purchased must be carefully considered as differences in efficiency of merely a fraction of one percent can greatly affect the yield of the entire system.

The efficiency is also a very important factor for the controllability of power electronics applications as every loss in efficiency also means power dissipation, which is directly converted into heat.

The higher the system performance, the higher the effort for removing the generated power dissipation. Higher power dissipation also means higher economic losses caused by the low efficiency of the entire system.

# **Challenges for Electronic Substrates**

Electronic substrates for power electronics applications must support the requirement for a high efficiency of the entire system. Therefore, the losses on this level must be minimized.

The second requirement is the support for thermal management of the assembly, in which the electronic substrate often plays an important role.

In addition to that, electronic substrates in power electronics must obviously support all functions of electronic substrates in conventional electronics.

6 Electronic substrates for power electronics applications must support the requirement for a high efficiency of the entire system.

# **Impact of Materials**

# **Losses in Metal Layers**

Ohmic losses in metal layers that often consist of copper or copper alloys play an important role in power dissipation considerations for electronic substrates. Even though the intrinsic resistance of copper is low, it cannot be ignored if high currents are present, as it causes the conductor to heat up. This contributes to heat development in the entire system and must therefore be minimized.

# **Properties of Insulators**

Another important factor in these considerations is the thermal conductivity of the substrate: The ampacity of a conductor is ultimately limited by the thermal destruction of the conductor. The better the heat dissipation of the conductor itself, the more current it can carry. Therefore, factors such as the specific thermal conductivity and thickness of the insulator play a crucial role.

# **Increasing Conductor Cross-sections**

Increasing the conductor cross-section is an effective method to reduce the ohmic resistance. In many cases, there is no alternative to this. However, it must be considered that increasing the cross-section leads to additional weight, which is undesired in electric mobility applications as any increase in weight decreases the driving range of the electric vehicle. The conductor cross-section design must in turn satisfy the specifications regarding heat generation. The heat generation depends on the thermal conductivity of the substrate and its connection to a suitable heat sink. The higher the temperature stability of the insulator, the higher the permissible heat generation in the conductor for system design.

For these reasons, determining the required conductor cross-section has evolved into a complex task. The conventional methods and rules for layout design as described in IPC or FED can no longer be applied in many cases as they do not take these new boundary conditions into account.

### Temperature Stability of Substrates

Another central aspect is the temperature stability of PCB substrates in power electronics. Power semiconductors can usually withstand junction temperatures of 175°C. This temperature range is increased further by new semiconductor technologies and is expected to reach 200°C or even 225°C within the next few years.

The full exploitation of this temperature range requires substrates that can be used in the mentioned temperature range.

Increasing the operating temperature also serves the purpose of minimizing efforts for the cooling system and hence minimizing system costs of the power electronics.

Ceramic substrates such as DCB/DBC substrates currently have a deep impact on power electronics as they combine excellent electrical insulation with high thermal stability. The downsides are the high costs of ceramic substrates and the limitation with regard to fine structures and number of substrate layers.

Organic PCB materials do not have these restrictions with regard to structure and number of layers, however, the thermal conductivity of the epoxy resins used is significantly lower than in ceramic materials.

A big advantage of PCB substrates is their significantly lower cost, which is why the use of ceramic substrates is limited to those power electronics that cannot be implemented without the properties of ceramic materials.

### Assembly and Interconnection Technology for Power Electronics Systems

The conventional processing technology for PCBs is the fully automatic assembly of SMD components. The through-hole assembly is mostly limited to DC-link capacitors, if these have not yet been replaced by SMD components.

In ceramic substrates, the bottom side of bare semiconductors is connected to the substrate in the electrical, mechanical and thermal sense by means of conductive adhesives, soldering, silver sintering or diffusion soldering.

The conventional way of connecting the top side is via aluminum heavy-wire bonding, how-

ever, this technique is slowly being replaced by Cu wire bonding. After assembly, the bonds are often stabilized by sealing them with a highly viscous silicone gel.

The required logic control and driver electronics are implemented via a separate substrate (usually a PCB) and are often interconnected with the power electronics via press-fit contacts.

Most entire systems of power electronics applications have a large number of different assembly and interconnection technologies that must meet the required targets regarding reliability and costs on their own as well as in combination.

## **Reliability Aspects of Assemblies**

#### Adjustment of the Expansion Coefficients

Due to their coefficient of expansion (CTE), organic PCBs are well-adjusted for components in housings such as QFP or DIP. Assembly of bare semiconductor components such as flip chips, however, is critical. Depending on their structural design, ceramic chip capacitors can also be critical as they have significantly lower CTEs.

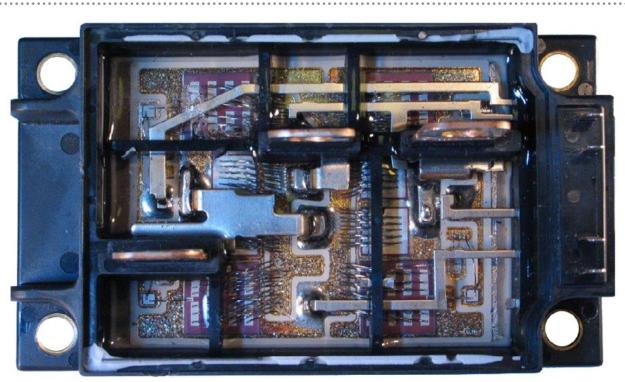
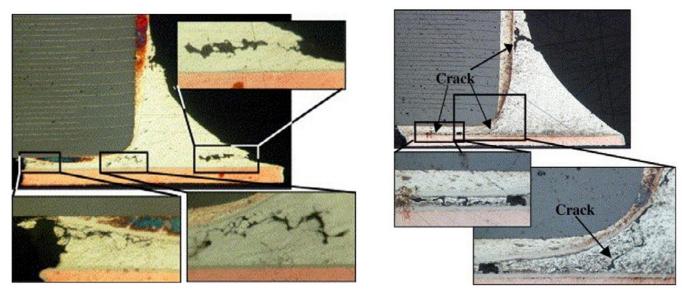


Figure 1: IGBT module power electronics based on DCB ceramics with power busbars in plastic housing. (Source: www.enacademic.com)



Figures 2 and 3: Soldered joint failure of a ceramic chip capacitor.

As opposed to that, DCB/DBC ceramics are assembled with bare power semiconductors. The lower coefficient of expansion of the ceramic base material leads to a better adjustment of the CTE between substrate and component in this scenario. The bare dies are then connected to the substrate and the terminals using wire bond technology. Due to their ampacity, heavy aluminum wires with a diameter of 500–600 µm are used for this.

# Failure Mechanisms of Assemblies

The classic failure of assembled PCBs is failure of soldered joints in poorly adjusted components due to cyclic thermal loads. In the PCB itself, failure of interconnections has to be mentioned, due to the anisotropy of the CTE in x/y direction as compared to the z direction is common.

In ceramic assemblies, however, the classic failure case is bond lift-off from the power semiconductor caused by the large difference in the CTE between Si (2.7 ppm/K) and Al bond wire (24 ppm/K). Another mechanism is conchoidal fractures of ceramics induced by CTE differences of ceramics (approx. 7 ppm/K) and copper metallization (17 ppm/K).

Due to the aforementioned reasons, most power electronics systems use a mixture of ceramic substrates and PCBs that are interconnected by assembly and interconnection technologies that can be very sophisticated and

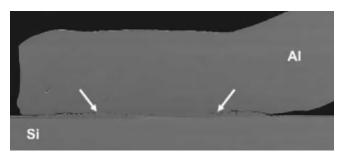


Figure 4: Cracks in a heavy wire bond on an IGBT (silicon) surface. (Source: www.powerguru.org)

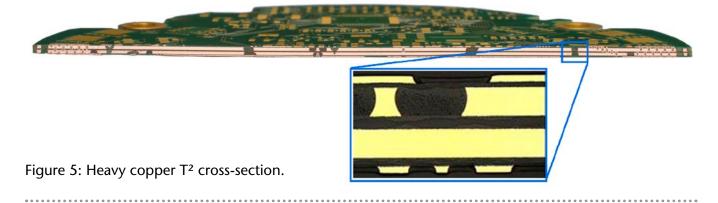
complex at times. They are implemented by way of wire bonding, plug connectors, soldering or welding technologies, and modern power electronics systems often combine all available assembly and interconnection technologies in one single system.

# **Optimization of Power Electronics Systems**

Therefore, the essential requirements for optimized substrates in power electronics systems are as follows:

- Increased ampacity
- Optimized thermal conductivity
- Increased temperature stability
- Reduced system complexity
- Increased system reliability
- Minimized costs





# Solutions for Today's and Tomorrow's Requirements

#### **Heavy Copper T<sup>2</sup>**

Heavy Copper T<sup>2</sup> is based on conventional heavy copper technology. In conventional heavy copper technology, the PCB design is characterized mainly by etched areas that must be filled with large resin volumes released by the prepregs used during the lamination process. Due to the large amount of resin used, multiple prepregs must be used, leading to large insulation thickness between the outer layer and the inner heavy copper layer. This means that the microvia technologies such as laser-drilled blind holes could not be used with heavy copper technology due to the large insulation thickness. Furthermore, the insulation thickness increases the thermal resistance of the printed circuit board and decreases its reliability as interconnections of thicker circuits are subject to more stress during cyclic thermal loads.

Heavy Copper T<sup>2</sup> technology overcomes these disadvantages by filling the etched areas of heavy copper circuits in a special manufacturing step. Therefore, thin prepregs can be used in the subsequent lamination process. This results in the following advantages:

- Lower overall thickness of the printed circuit board
- Lower clearances between the copper layers
- Increased reliability in cyclic thermal loads
- Increased thermal conductivity in the Z-axis (through plane) of the design



Figure 6: Cross-section of the Power Combi Board.

#### **The Power Combi Board**

The Power Combi Board uses a combined inner layer with heavy copper areas used for highcurrent conduction. However, the same level also has copper layers with a standard thickness of 18 or 35 µm that help to ease the routing for the use of complex components.

With this technology, the power and logic parts of an application can be implemented with just one circuit board, whereas previously, two circuit boards were necessary, which had to be connected with a plug connector.

The new solution helps increasing the reliability and making optimal use of the required installation space.

#### **The Inlay Board**

Printed circuit boards with pressed-in copper coins are well-known in the area of thermal management. The main disadvantage of this technology is the challenging thickness adjustment of the copper coins to the circuit board. While the coins have very low tolerances, multilayer circuit boards have a thickness tolerance of up to 10% due to the manufacturing processes. Therefore, flush fitting of the circuit board

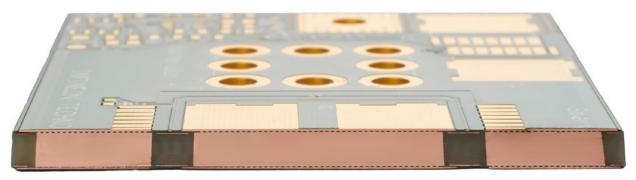


Figure 7: Inlay board with copper inlays of 2 mm thickness.



Figure 8: Lead frame with cavities for assembling power semiconductors.

surface with both sides of the inlay surface is only possible in a part of the manufactured lot. This can lead to varying thicknesses of the thermal interface material used during heat sink installation.

The inlay technology from Schweizer is different as the inlays are not pressed into a finished circuit board but are laminated into the assembly group as part of a multi-layer manufacturing process. In this process, the prepregs used equalize the occurring differences in thickness between inlay and circuit board.

The inlay can be entirely embedded in the matrix, leading to an electrically insulated inlay or it can be installed flush with one side of the entire structure of the circuit board, enabling it to be used for optimal thermal transition.

As the inlay is usually significantly wider than the component assembled on it, an immediate heat dissipation takes place within the inlay. This enlarged transition area at the heat sink leads to lower thermal resistances in the area of the thermal interface material.

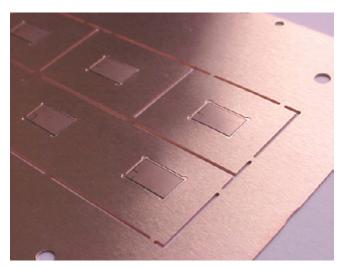


Figure 9: Lead frame with assembled MOFSETs.

Apart from thermal management, such inlay circuits can also be used for conducting high currents at low ohmic losses.

Most applications utilize the low ohmic losses as well as the optimized thermal interconnection to the heat sink, which is why the inlay board represents a high-end solution based on conventional printed circuit boards.

# The Smart p<sup>2</sup> Pack

The precondition for miniaturization of high power electronics is a significant reduction of losses within the circuit and the efficient removal of power dissipation from the confined space. The p<sup>2</sup> Pack technology enables super-flat power modules with a thickness of 1–1.4 mm with reduced power dissipation and improved switching behavior as a result of using embed-

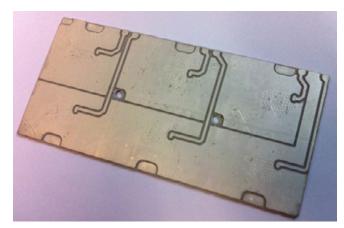


Figure 10: Connection of gate/source pads with conductor track structures.

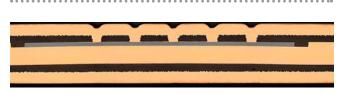


Figure 11: Cross-section of a p<sup>2</sup> Pack with Cu-filled microvias.

ding technology and processes from the printed circuit board industry.

With the  $p^2$  Pack technology, an entirely new technology for manufacturing power modules has become available. So-called lead frames form the basis for this technology. These lead frames are machined to provide cavities for the assembly of power semiconductors.

In the next step, these cavities are assembled with power semiconductors. The goal is to position the surface of the semiconductors in one level with the lead frame.

The assembled lead frames are laminated with the help of conventional PCB processes to form a 3-layer structure. This way the bond wires are replaced by a circuit board wiring layer above the chip. The gate contact is implemented with conductor tracks and the source pads have a flat design in order to achieve an electrical connection as well as favorable thermal dissipation of the power.

Contacting the upper side of the chips is done galvanically by way of copper-filled blind holes penetrating through the dielectric on the

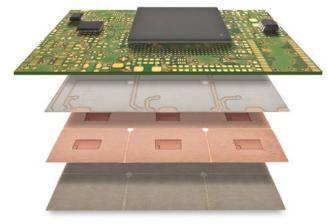


Figure 12: Exploded drawing of the Smart p<sup>2</sup> Pack functional layers.

upper side. The semiconductors must have a surface metallization that is compatible with these processes.

The design of the  $p^2$  Pack is to be kept symmetric as it ensures a minimized pumping effect during thermal cycles. The solid Cu-layers above and beneath the lead frame are a design feature for double-sided cooling of the semiconductor while only the lower side must be connected to a heat sink. Depending on the lead frame thickness, up to 1/3 of the dissipated power can be distributed via the upper side and can be removed downwards through the package into the heat sink.

#### Smart p<sup>2</sup> Pack

The  $p^2$  Pack itself can be combined with a logic control board to form a 1:1 substitute for a DCB substrate.

Due to the fact that the  $p^2$  Pack has a height of only 1 to 1.4 mm, it can even be embedded in a logic control board. Very short connections between the gate driver and the gate contacts of the power semiconductors can be achieved this way. The driver module can be positioned on the control board directly above the power semiconductor while the connection to the gate is carried out with copperfilled interconnections from the outer layer to the  $p^2$  Pack.

A heat sink can be mounted on the bottom of the Smart  $p^2$  Pack using a thermal interface material.

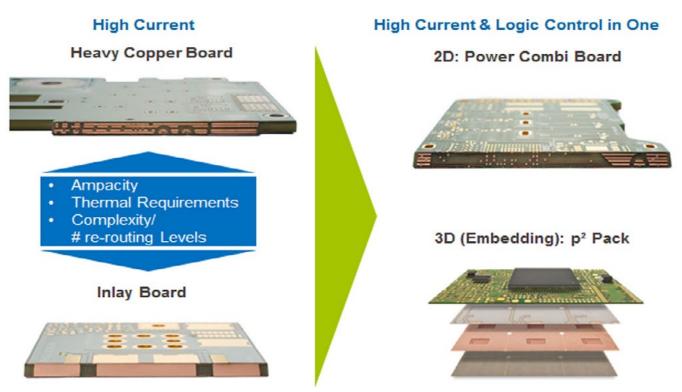


Figure 13: Overview of requirement and solution concepts.

# Which technology is suitable for which task?

The technology to be used is determined by the requirements of the application.

For example, the number of grids carrying high currents determines whether a heavy copper board (many grids) or an inlay board (few grids) will be used.

If a combination of logic and power circuitry is to be implemented in a single circuit board, the Power Combi Board is available for this purpose.

The Smart p<sup>2</sup> Pack is the perfect solution if very limited installation space is available, circuit losses must be minimized and maximum electric and thermal performance is required in limited space.

# Summary

Power electronics have entered the high-volume market as a result of increased electrification of the power train and auxiliary units in motor vehicles. This has pushed the demand for miniaturization and cost reduction as an electric drive has to be installed in addition to the combustion engine and as many useful additional electric auxiliary units must be installed in the installation space that has always been very limited.

This trend requires electronic substrates capable of handling very high electric power at very low losses. Due to the limited installation space, locations with high ambient temperatures must be used as well, resulting in more demanding temperature requirements.

With the new highly temperature-resistant materials and high-current technologies described, future applications can be increasingly based on circuit board technology. **PCB** 



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